

# Monolithically Integrated Rad-Hard SiC Gate Driver for 1200 V DMOSFETs, Phase II

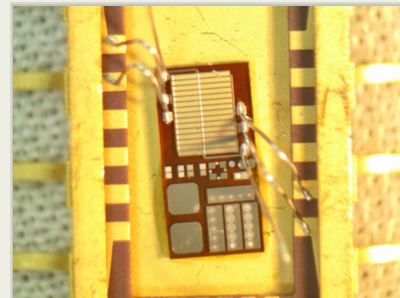
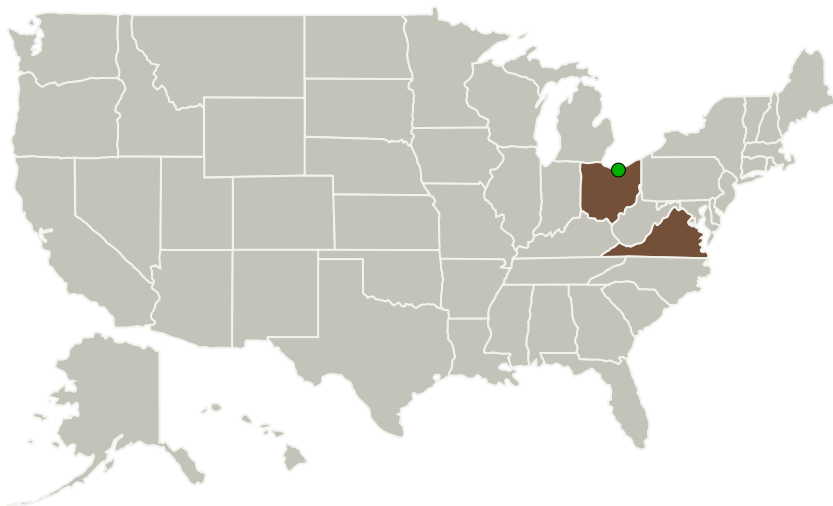
Completed Technology Project (2017 - 2019)



## Project Introduction

This two-phase SBIR program targets the need for highly integrated SiC-based electronics systems by developing gate drive circuitry that can be fully integrated with 4H-SiC power switching devices, enabling eventual realization of a monolithic power switching platform. Specifically, the final goal of this program is to develop and demonstrate a fully integrated, isolated gate driver architecture, having an integrated SiC power MOSFET. In addition to integrated resistors and capacitors, development of SiC CMOS technology will entail the demonstration of lateral SiC NMOSFETs and the more challenging SiC PMOSFET devices with adequate performance and radiation hardness. During Phase I, an NMOS-only gate drive buffer circuit was designed and implemented on the same host substrate used for fabricating 1200 V SiC DMOSFETs. Phase II will focus on integrating the gate drive buffer IC fabricated during Phase I with a 1200 V rated power SiC DMOSFET. Process and device development of a SiC PMOS technology will be conducted during Phase II, in pursuit of a SiC CMOS gate drive circuit. The fabricated power and lateral SiC devices will be subjected to extensive radiation testing to investigate the degradation pathways of this monolithic power switching device, when exposed to high radiation environments.

## Primary U.S. Work Locations and Key Partners



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| Organizations Performing Work | Role                    | Type  | Location         |
|-------------------------------|-------------------------|---|------------------|
| GeneSiC Semiconductor Inc.    | Lead Organization       | Industry<br>Minority-Owned Business, Small Disadvantaged Business (SDB) | Dulles, Virginia |
| ● Glenn Research Center(GRC)  | Supporting Organization | NASA Center   | Cleveland, Ohio  |

## Primary U.S. Work Locations

|      |          |
|------|----------|
| Ohio | Virginia |
|------|----------|

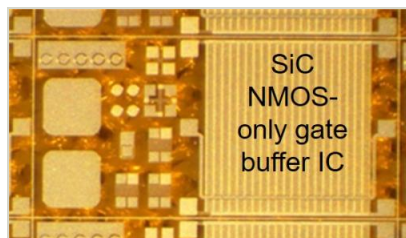
## Project Transitions

**June 2017:** Project Start**December 2019:** Closed out

### Closeout Documentation:

- Final Summary Chart(<https://techport.nasa.gov/file/140856>)

## Images



### Briefing Chart Image

Monolithically Integrated Rad-Hard SiC Gate Driver for 1200 V DMOSFETs, Phase II Briefing Chart Image  
(<https://techport.nasa.gov/image/127105>)

## Organizational Responsibility

### Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

### Lead Organization:

GeneSiC Semiconductor Inc.

### Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

## Project Management

### Program Director:

Jason L Kessler

### Program Manager:

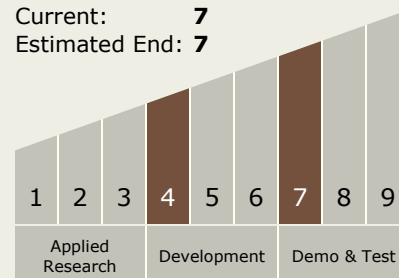
Carlos Torrez

### Principal Investigator:

Ranbir Singh

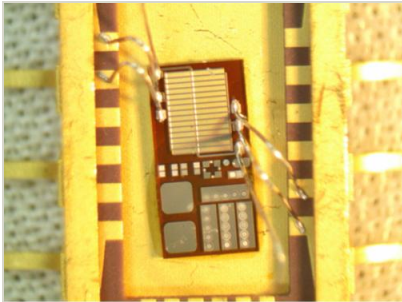
## Technology Maturity (TRL)

Start: 4  
Current: 7  
Estimated End: 7



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## Final Summary Chart Image

Monolithically Integrated Rad-Hard  
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(<https://techport.nasa.gov/image/135032>)

## Technology Areas

### Primary:

- TX03 Aerospace Power and Energy Storage
  - └ TX03.3 Power Management and Distribution
    - └ TX03.3.1 Management and Control

## Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System